



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Taylor R. Efland, et al.

Art Unit: 2812

Serial No.: 10/725,642

Examiner: TBD

Filed: 12/02/03

Docket: TI-32451

For: Low Cost Fabrication Method for High Voltage, High Drain Current MOS Transistor

**LETTER TO THE OFFICIAL DRAFTSPERSON**

**MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)**  
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service on 3-8-04 as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Karen Vertz  
Karen Vertz

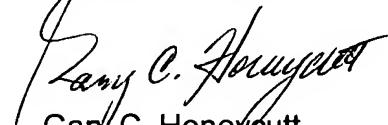
3-8-04  
Date

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Enclosed are **SIX (6)** sheets of formal drawings for the above-referenced case. Please charge any necessary fees to Deposit Account No. 20-0668 of Texas Instruments Incorporated. This sheet is enclosed in triplicate.

Respectfully submitted,

  
Gary C. Honeycutt  
Reg. No. 20,250

Texas Instruments Incorporated  
P.O. Box 655474 M/S 3999  
Dallas, Texas 75265